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Chapter 12

RECTIFYING AND CLAMPING CIRCUITS

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CHAPTER 12

RECTIFYING AND CLAMPING CIRCUITS

1. RECTIFICATION

A description of the process of rectification (and detection) is given in the Radio books of three Services. However, certain principles of rectification are discussed here, since they form the basis of a knowledge of Clamping, and it is desirable that the connection between the two processes should be clear.

A rectifying or detecting circuit is shown in Fig. 574(a). Assume for simplicity that the applied voltage v_i has the rectangular waveform shown in Fig. 574(b) and that its amplitude is denoted by $\hat{v}_i$.

At the start of the operation the condenser C is uncharged and the voltage across it is therefore zero. At the beginning of interval (1) the applied voltage rises suddenly from zero to $\hat{v}_i$. This change of voltage appears instantaneously across the diode, which then conducts strongly. Hence C charges through the diode, and the voltage across it rises with a time-constant CR_D towards $\hat{v}_i$ (Fig. 574(c)). (R_D is the resistance of the diode when this valve is conducting.) During interval (1) the voltage across the condenser rises to V'. Simultaneously, the voltage across the diode falls to $(\hat{v}_i - V')$ (Fig. 574(d)), since at any instant the sum of the voltages across the condenser and across the diode must equal the applied voltage.

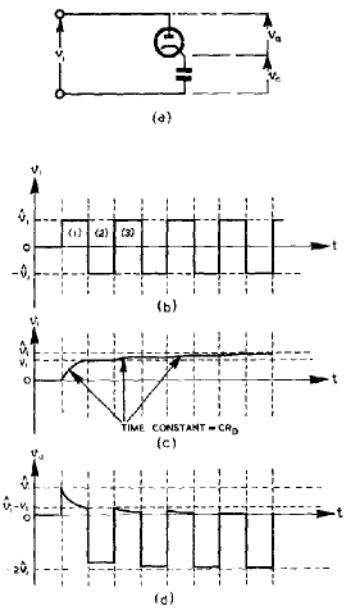


Fig. 574. - Action of simple rectifying circuit.

At the end of interval (1) the applied voltage falls suddenly by an amount $2\hat{v}_i$. This voltage change appears instantaneously across the diode, and consequently the current is cut off. Since no current flows in or out of the condenser C, the voltage across C remains constant. So long as the applied voltage remains steady (interval (2)), the voltage across the diode does not vary.

At the beginning of interval (3) the applied voltage, and therefore the voltage across the diode, rises suddenly by an amount $2\hat{v}_i$. The diode conducts as soon as the input voltage across it reaches V'. Consequently, the voltage across the condenser rises exponentially, with time-constant CR_D from V' towards $\hat{v}_i$ (interval (3). The rise of voltage across the condenser C during interval (3) is not so great as during the equal interval (1), since the voltage range over which the condenser tends to charge is smaller. The voltage across the diode falls during interval (3) by the same amount as the voltage across the condenser rises.

The voltage v_c across the condenser eventually reaches a value $\hat{v}_i$ at which it remains. The voltage across the diode then has a mean value of $-\hat{v}_i$ i.e., the peak voltage is zero. A similar result is obtained if the applied voltage is sinusoidal.

In practice the voltage developed across C is the output of the rectifier circuit, which is normally used as a source of steady voltage for other circuits. The load on the rectifier due to these other circuits taking current can be represented by a resistor R connected in parallel with C, (Fig. 575(a)). Under such circumstances the operation of the circuit is modified since C can discharge through R.

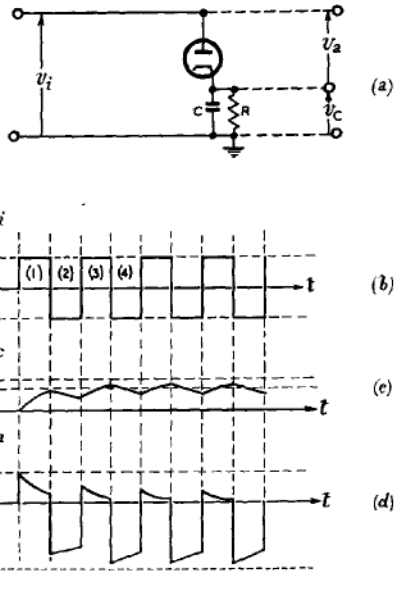


Fig.575.- Action of practical rectifying circuit.

Assuming, as is normal with a rectifying circuit, that R is large compared with R_D, C charges with time-constant approximately equal to CR_D, during the time the diode conducts. When the diode is not conducting C discharges with time constant CR. As in the case of an alternating voltage applied to a series C-R circuit (see Chapter 2 Sec.4) the circuit eventually settles down to a steady state in which the charge accumulated on C during each cycle is equal to the charge which leaks away through R (Fig.575(c)). From then onwards the voltage across the condenser fluctuates, during successive cycles, about a constant value $\bar{v}_C$, slightly smaller than v_i. The greater is the value of R compared with R_D the more closely does the mean value of the voltage across the condenser approach to $\hat{v}_i$, and the smaller the amplitude of the fluctuations about this mean value.

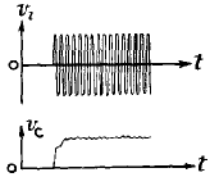


Fig.576.- Detection of CW oscillations.

The above discussion applies also to the detection of amplitude-modulated CW. Fig.576 illustrates a CW oscillation which is to be detected by the circuit of Fig.575a. Provided the time-constant CR is much longer than the period of oscillation the steady value of the voltage across the condenser is almost equal to the amplitude of the applied voltage. If the oscillation (frequency f_o) is amplitude

modulated (modulation frequency f_m), as shown in Fig. 577, then, provided $\frac{1}{f_o} \ll CR \ll \frac{1}{f_m}$ the voltage across the condenser, at any instant, conforms almost exactly to the shape of the modulation envelope.

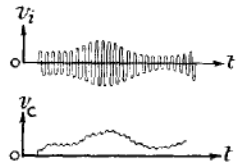


Fig. 577.- Detection of amplitude modulated CW oscillations.

In radar equipments the voltage applied to the detector circuit takes the form of radio-frequency pulses as shown in Fig. 578. Such a voltage may under certain circumstances be considered as an extreme form of that shown in Fig. 577. If the voltage across the condenser is to conform faithfully to the pulse shape it is necessary that $\frac{1}{f_o} \ll CR \ll T$, where T is the duration of the pulse.

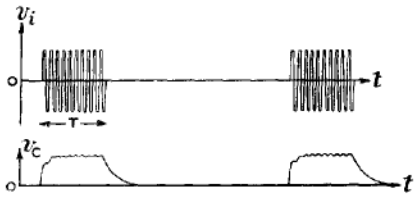


Fig. 578.- Detection of RF pulse.

2. SIMPLE CLAMPING CIRCUITS

So far, in the discussion of the operation of the circuits shown in Figs. 574 and 575, the emphasis has been on the form of the voltage across the condenser. However, it has been pointed out that the voltage developed across the diode is almost entirely in one sense only. If one of the electrodes is connected to a source of constant voltage the voltage at the other electrode is prevented from either rising above or else falling below this fixed level according to the method of connection. This process is known as Clamping. Various other terms are used to describe clamping, depending on the nature of the input voltage variations.

If the input consists of a succession of unidirectional pulses, either all positive-going or all negative-going, and the output is clamped so that the base-line is at a fixed level independent of the amplitude of the pulses, the process is called Base-line Stabilisation. If, on the other hand the peaks (of either the positive-going or the negative-going positions) are clamped, the term Peak Level Stabilisation is used. The term DC Restoration also is frequently used to describe these processes, but strictly should be reserved for the case in which the mean level of the output voltage is made the same as that of the input. Common examples of radar circuits utilising peak-level stabilisation are those employing valve switching or "gating" pulses or slide-back biasing arrangements (Chapter 7). Where gating pulses are applied to release the bias on either the suppressor or the control grid of a valve it is usually necessary to ensure that the level at which the grid is held during the conducting period should be clearly defined. This may be achieved by grid current flow, but the addition of a diode usually facilitates clamping. Examples of this form of clamping are to be found in Chapters 10 and 11.

Base-line stabilisation has common application to CRT circuits. For example, in PPI systems, where the signal pulses are usually applied to the grid or cathode via a C-R network, it is important that an increase in the amplitude of some signals should not depress the general level of

the brightness and so make weaker signals ineffective. If the base-line is clamped at a predetermined level, the amplitude of signal necessary to cause an indication on the screen is constant. Clamping is also commonly employed in time-base circuits and in deflection systems using a simple A-display. Consider the latter case, in which the signal pulses are applied via a C-R circuit to the Y-plates to produce the trace shown in Fig. 579 . An increase in the mean signal amplitude would, in the absence of any clamping device, cause the base-line to be depressed. If this is undesirable, a clamping diode is usually employed to ensure that the base-line occurs at a fixed position on the screen.

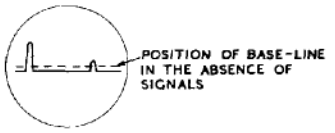


Fig.579.- Shift of base-line in presence of signal.

The simplest type of clamping circuit is shown in Fig. 580 . So far as the voltages across C and the diode are concerned, the operation of this circuit is essentially the same as that of the circuit shown in Fig. 575a

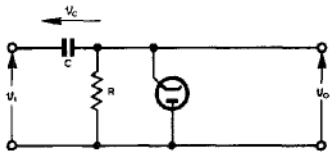


Fig.580.- Simple circuit for clamping negative-going excursions of output voltage.

Consider first the effect of applying to this circuit in the absence of the diode the input voltage variation shown in Fig. 581a (This is the type of output commonly obtained from the anode of a pulse-amplifying valve). Provided the time-constant CR is long compared with the repetition period of the input pulses, the output voltage in the steady state takes the form shown in Fig. 581(b). The voltage developed across C is shown at (c); (compare Chapter 2 Section 4).

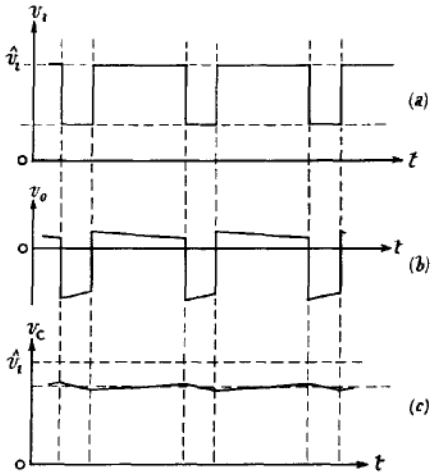


Fig.581.- Action of circuit of Fig.580; diode out of circuit.

If the voltage variation of Fig. 581(a) or 582(a) is applied to the circuit of Fig. 580 , this time with the diode in circuit, the circuit conditions settle down to the state depicted in Fig. 582(b) and (c). In the steady state the peaks of the negative-going pulses are clamped at zero potential. The condenser is charged to approximately $\hat{v}_i$. Since $CR \gg T$, only very little additional charge is acquired while the input is at $\hat{v}_i$, the diode being non-conducting, so that the condenser

voltage v_c rises by only a small amount. When the input falls again to $\check{v}_i$ the diode conducts and the additional charge rapidly leaks away and v_c falls again to $\check{v}_i$.

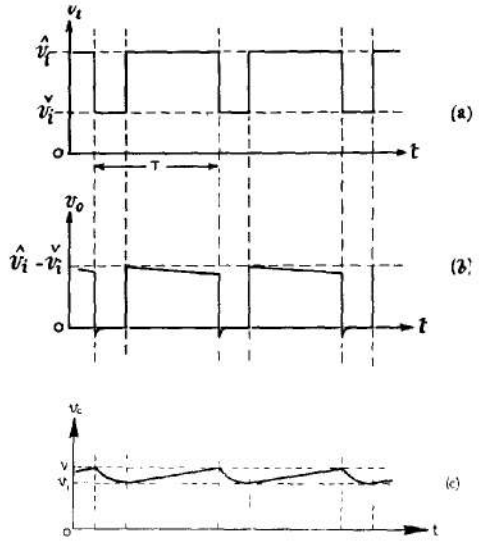


Fig. 582. - Action of circuit of fig. 580; diode in circuit.

The effect of such a circuit in practice may be even more pronounced than has already been indicated, owing to the low value of the input resistance of the circuit when the diode is conducting. This occurs in the arrangement shown in Fig. 583(a). In the absence of the diode, the output voltage shown at (c) is developed across R in response to the input shown at (b) When the diode is in circuit, the output voltage settles down to the steady state shown at (d).

The action of the circuit of Fig. 583(a), with the diode inserted, is as follows.

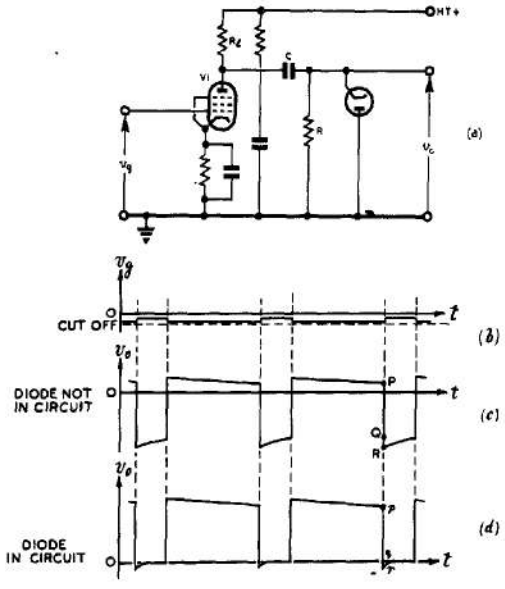


Fig. 583. - Effect of low input resistance of diode.

While the diode is not conducting no change in the amplitude of the output voltage variation occurs, so that pq (d) is equal to PQ (c). During the conducting period the input resistance to the clamping circuit is very small (R_D), and since this is effectively in parallel with the anode load the amplification is substantially reduced. This causes the negative-going peak qr (d) to be very much less than the corresponding peak QR (c), so that the clamping effect is considerably enhanced.

Fig. 584a shows the diode circuit in a form suitable for clamping the positive-going extremities of the output voltage. The steady state conditions are illustrated in Fig. 584 . The condenser charges during the positive-going excursions of the input to approximately $\hat{v}_i$, discharging slightly during the negative-going excursions. This causes the output voltage to rise slightly above zero potential at the beginning of each positive-going excursion, so that the diode conducts, and rapidly recharges the condenser to $\hat{v}_i$.

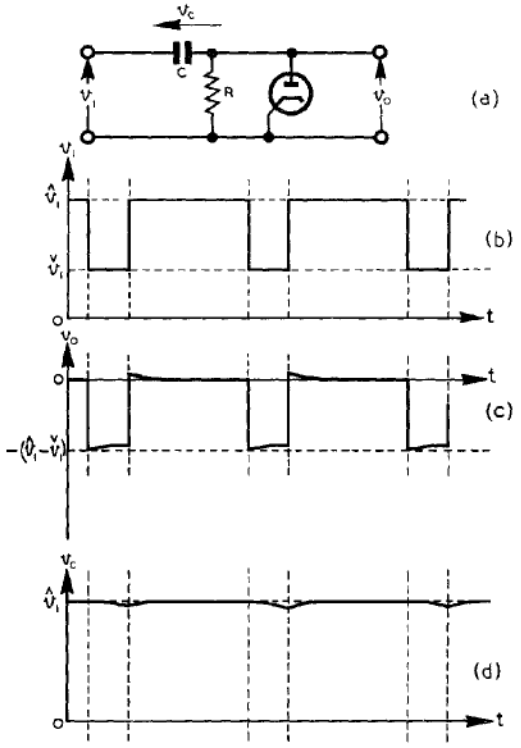


Fig.584.- Clamping of positive-going excursions of output voltage.

Clamping may be performed at the grid of a triode or pentode. Thus the grid of the valve shown in Fig.585 acts as the anode of a diode; any tendency for the grid voltage to rise above zero causes grid current to flow and the condenser C is charged rapidly. The arrangement shown is essentially that needed to obtain automatic bias by using the flow of grid current (see Chapter 7 Section 4). Clamping is an extreme form of such automatic biasing.

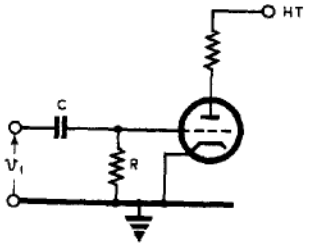


Fig.585.- Use of control grid for clamping

The circuits discussed above clamp one or other extremity of the output voltage to zero. However, clamping may occur at any other desired reference level. For example, Fig. 586(a) shows a circuit which is capable of clamping the upper extremity of the output at some positive level V. The steady state conditions of the circuit are illustrated at (b) and (c)

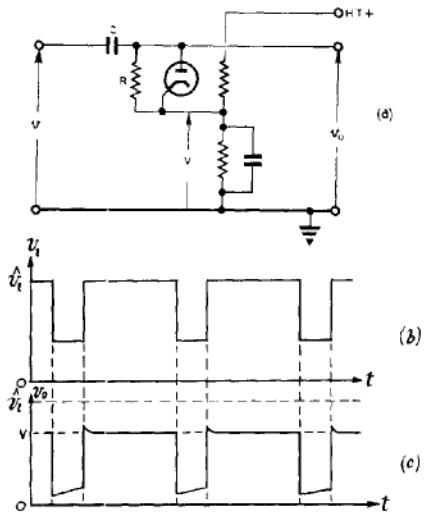


Fig.586. - Clamping at a level other than zero.

Clamping may also be applied to a time-base voltage. The necessity for such a procedure depends on the type of voltage variation and on the conditions under which it is used.

Fig. 587(a) shows a typical time-base voltage which has a discontinuous sawtooth waveform. If this voltage is applied, say, to a deflector plate of a CRT, via a C-R coupling circuit, the deflector plate voltage varies about a mean level represented by the line AB at (b). This mean level is usually determined by the setting of the shift control. It is often necessary, in radar apparatus, to change the duration of the time base, without altering the repetition frequency (Fig.587(c)). Figs.587(b) and (c) show how the change in time-base duration alters the level from which the time-base voltages rise , and so changes the starting position of the time-base on the screen of the CRT. Similarly, if there is a change in the amplitude of the time-base voltage as shown at (d) , there is again a change in the starting position of the time-base. Where changes of time base duration or amplitude are necessary it is clearly desirable to introduce clamping.

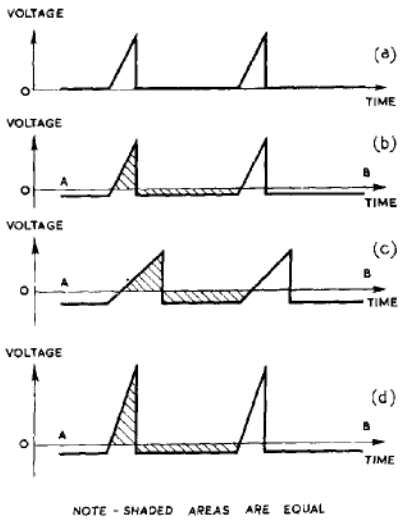


Fig.587. - Sawtooth pulses; effect of changing amplitude or duration.

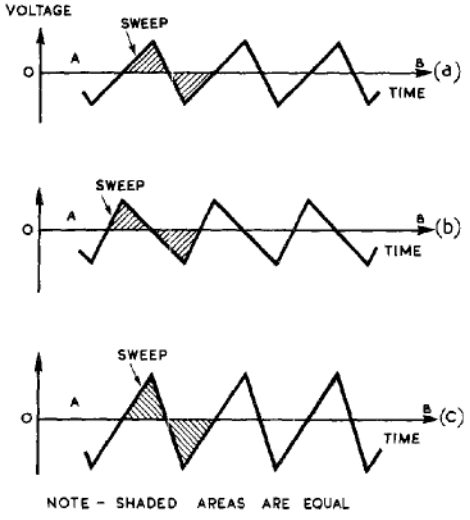


Fig.588. - Continuous sawtooth voltage; effect of change of amplitude or sweep-to-flyback ratio.

If the time-base voltage has a continuous sawtooth waveform, as shown in Fig. 588(a) conditions are rather different. For example, (a) and (b) represent time-base voltages of the same amplitude but with different sweep-to-flyback ratios. In these cases there is no difference between the voltage levels from which the time-base voltages rise. However, if there is a change in the amplitude of the time-base voltage, as illustrated at (c), there is a change in the starting voltage level, and therefore in the position of the start of the time-base on the screen of the CRT.

This may not be deleterious, since the mean value of the time-base voltage corresponds to the centre of the trace, which is usually positioned at the middle of the screen. The increase in amplitude causes the time-base to extend farther across the screen in both directions.

It may be desirable for the time-base to start from the centre of the screen of the CRT (e.g. PPI presentation), i.e., for the effective time-base voltage to rise from zero. This may be accomplished by clamping the lower level of the time-base voltage to zero, by one of the methods described in this chapter.

3. SWITCHED CLAMPING CIRCUITS

The circuits described in Section 2 are examples of a simple type of clamping in which one extremity of the output voltage is clamped at a fixed level. However, sometimes a different type of clamping is required, in which both positive-going and negative-going output pulses are made to start from some fixed level.

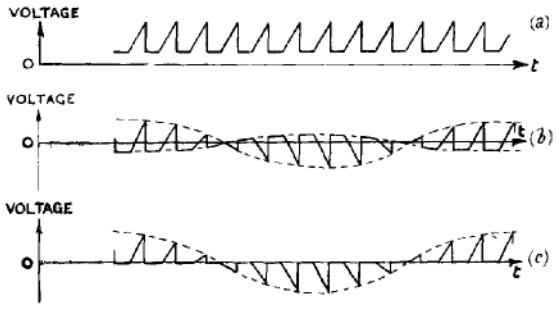
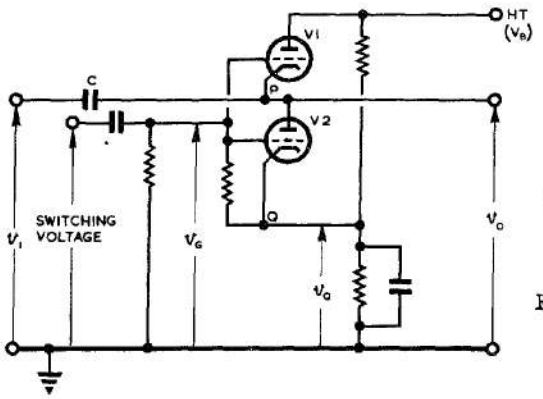


Fig. 589. - Voltage variation requiring switched clamping.

In Chapter 11 Section 13 a method of producing a rotating time-base is described. An essential part of the method is the use of a resolver (see Chap. 3, Sec. 19). A sawtooth voltage as in Fig. 589(a), is applied to the resolver and if a non-resistive resolver is used, output voltages of the form shown at (b) are obtained. The steady component of the applied voltage is lost in the resolver and each output pulse settles down about its mean value. As the sawtooth pulses change in amplitude the time-base voltages start from varying levels, and not from zero as is required. If all the time-bases are to start from the centre of the screen the output voltage should take the form shown at (c). The transformation of the waveforms from the form of (b) to that of (c) is accomplished by clamping the voltage during each interval between successive sweeps to a fixed value (i.e., zero). This requires that the clamping circuit should be switched into operation during these intervals only.

Fig. 590(a) shows a circuit arrangement for providing switched clamping. The output voltage is maintained at a steady value except for the time during which the clamping valves (valve 1 and valve 2) are rendered non-conducting by means of negative-going pulses, lasting throughout each time-base sweep, which are applied to the control grids of both valves. The relation between the switching pulses and the applied voltage is shown at (b) and (c).



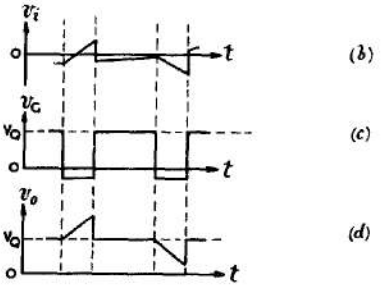


Fig.590.- Action of switched clamping circuit

Valves 1 and 2 are in series between the voltage levels V_B and V_Q (the voltage at Q). While the common grid voltage is held well below V_Q and v_o (which is also the voltage at P), neither valve is conducting the clamping circuit is inoperative. During the positive-going portions of the switching voltage (interval (a)) the grids are held at approximately V_Q, being clamped by the flow of grid current. The voltage at P then settles down to a steady value depending on the relative resistances of the two valves. This steady value cannot be greater than V_Q by an amount sufficient to cut off the current in valve 1. Hence, in the steady state, v_o would be stabilised a few volts above V_Q. As the input voltage v_i rises, v_o tends to rise, reducing the current in valve 1 so that the resistance of this valve is increased. This tends to reduce v_o and so counteracts the rise in input voltage. In the extreme case, when the rise in v_o is sufficient to cut off the current in valve 1, valve 2 acts as a clamping diode so that v_o is prevented from rising substantially above V_Q.

Similarly, if the input voltage falls the resistance of valve 1 decreases and tends to offset the fall in input voltage. If the voltage falls by an amount sufficient to cut off the current in valve 2, valve 1 acts as a clamping diode so that v_o is prevented from falling appreciably below V_Q.

The output voltage can be clamped at any desired level (below V_B) during the positive-going portions of the switching voltage by a suitable choice of the clamping level V_Q. In the application described the switched clamping circuit ensures that all the time-bases start from the same point. A potentiometer arrangement enables V_Q to be determined so that this point is brought to the centre of the screen.

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