Chapter 16

STATIC INVERTERS, ECKO, TYPES E182 and E184/1

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Introduction

1. The static inverters are designed to provide a 115V, 400 c/s a.c. output from a nominal 28V d.c. power supply. The Type E182 inverter is a single phase unit, and the Type E184/1 inverter is made up of two Type E182 single phase units coupled together to produce a 3-phase output.

DESCRIPTION

Inverter, Type E184/1

2. The inverter has four separate assemblies, comprising two standard Type E182 single-phase inverters, a 3-phase coupler unit and a mounting tray. The two Type E182 inverters are fitted in the composite mounting tray which interconnects the inverters and the 3-phase coupler unit to give a balanced 3-phase output. Cooling air to the side walls of both inverters is provided by a blower fitted to the coupler unit and supplied from the 3-phase output.

Inverter Type E182

3. The components of the inverter are housed within a rectangular metal case. A 10-way Cannon fixed plug is fitted at the rear end of the case for connection to the coupler unit. Access to the components is gained by removal of the top covers which are secured by the twenty 6 B.A. screws (A in fig. 2).

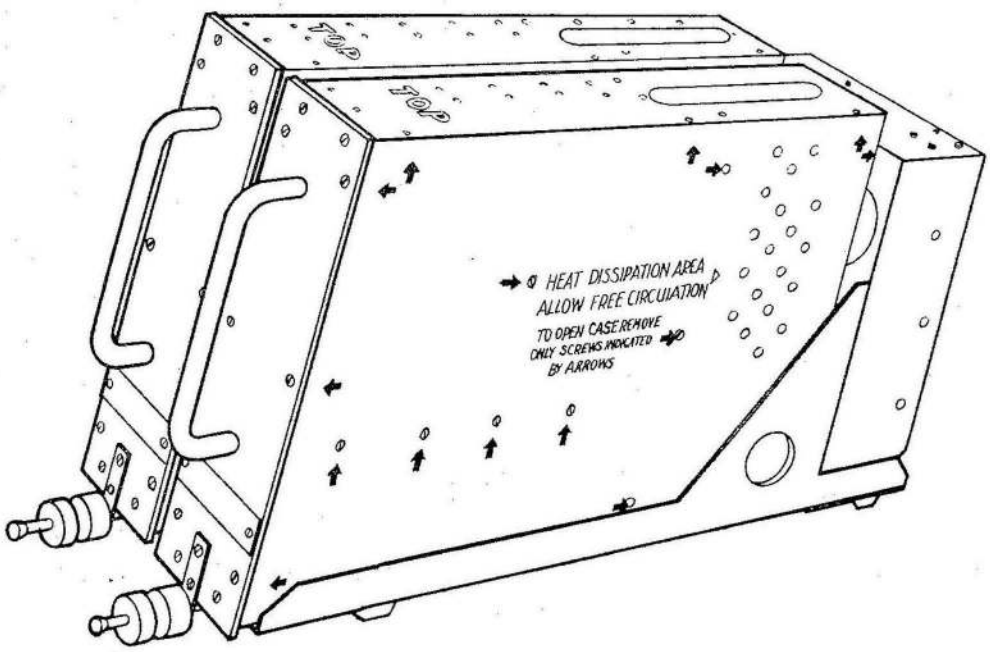

Fig. 1. General view of coupled units

Circuit description and operation

4. The circuit comprises a master oscillator operating from a stabilised d.c. line, with buffer stages which shape the drive waveform applied to the output transistors, a power amplifier which feeds power to the load via a tuned transformer, a voltage regulator and two protection circuits.

5. *Master oscillator.* Transistor VT1, transformer T1 and associated components are connected as a 400 c/s sine-wave oscillator, with the frequency fixed by a tuned circuit formed by capacitor C1 and the primary inductance of transformer T1. The variable pot core of T1 provides for continuous incremental adjustment of the nominal frequency. The oscillator provides an output of approximately 11V peak-to-peak to the base of transistor VT2. A section of T1 is also brought out to the plug PL1 for external synchronizing purposes. Transistor VT1 is biased by the potentiometer R3, R2 and the emitter resistor R1 so that the effects of variations in transistor gain are reduced. Transistor VT2 is an emitter follower to reduce the loading of the following push-pull transistors VT5 and VT6 on the oscillator circuit.

6. Transistors VT5 and VT6 are driven in anti-phase from transformer T2 secondary, so that they only conduct over part of the negative half cycle of the sine waves applied to their bases. The waveform across the primary of transformer T3 in the collector circuits thus consists of positive and negative part sine waves, with a wait period at cross-over. Two anti-phase secondaries on transformer T3 drive two further transistors VT7 and VT8. These transistors are unbiased and thus conduct only on the negative half cycles of the drive waveform, which are of sufficient amplitude to saturate the transistors and effectively connect the bases of transistors VT9 and VT10 to a 14V supply via the resistors R13 and R15.

7. A base current of approx. 50 mA is thus applied to transistors VT9 and VT10 in turn, causing saturation and producing a square wave output which is applied to the driver transformers T4 and T5 in the collector circuits. The primaries of transformers T4 and T5 are shunted by resistors R16 and R17 in series with diodes MR2 and MR3 to damp the over-swing generated by the square wave drive. Capacitors C6 and C7 provide a current reservoir for transistors VT9 and VT10 emitter supply.

8. *Power amplifier.* Transformers T4 and T5 supply the base currents for the eight output transistors, VT12 to VT19, connected in four parallel pairs to provide the required

rating. The phasing of the base currents is arranged so that on one half-cycle the current flows from choke L1 through transistor VT13, then through the primary of transformer T6 and back to the supply via transistor VT14. On the next half-cycle current flows through transistor VT15, transformer T6 primary and transistor VT12, but the direction of current flow through T6 is reversed. Transformer T6 is tuned by capacitors C10 and C13 to resonate at 400 c/s and thus converts the square wave primary current to a sine wave voltage output. The output winding is centre-tapped and also has a 100V tap both of which are brought out to plug PL1. The power supply to the bridge is connected through the choke L1 which, by interposing an impedance between transformer T6 and the d.c. power supply, allows a sinusoidal voltage to be developed across T6. In order to limit the voltage developed when the current through L1 is suddenly stopped, a diode MR5 is connected between the positive line and an anti-phase section of the winding on L1. When the voltage developed in this winding exceeds the supply voltage MR5 conducts and prevents any further rise. Capacitor C9 ensures that any transient voltage developed across L1, when none of the output transistors is conducting, is divided equally between the output transistors.

9. The circuit comprising capacitor C8, diode MR4 and resistor R18 is to prevent avalanche breakdown of the bridge transistors. When current through the bridge is switched off the voltage across L1, limited by MR5, rises rapidly to its peak value and, to reduce the rate of rise, the bridge current is transferred to C8 via the diode MR4. Resistor R18 limits the peak current drawn from C8 when the transistors are switched 'ON' and also discharges C8 in readiness for the next cycle.

10. *Voltage regulator.* The voltage regulation is achieved by rectifying a portion of the output, comparing it with the voltage across the Zener diode in a comparator bridge circuit, then feeding it back as a control bias voltage. Changes in bias affect the duration of the drive waveform relative to the wait period and thus control the output voltage.

11. Transformer T8 primary is connected across the output of the inverter and provides a secondary voltage of approximately 30V when the input, i.e. the inverter output, is 115V. This is rectified by diodes MR6 and MR7, and applied to the comparator bridge formed by resistors R19, R20, R21, RV1 and Zener reference diode MR10. The bridge output is then used to bias the control transistors VT3 and VT4. Transistor VT3 is connected as an integrator and VT4 as an emitter follower providing low impedance to feed the base circuit of transistors VT5 and VT6. The collector of VT4 is returned to the junction of resistors R9 and R29 to prevent the possible occurrence of a reversed loop condition when starting up. The bias control voltage, and hence the inverter output voltage is adjusted and pre-set by RV1.

12. *Overload protection circuit.* Each of the three primary windings on a further transformer T7, is in series with one of the inverter outputs to form part of an overload protection circuit. Transformer T7 secondary winding is fed into the comparator bridge arranged so that when the inverter is fully loaded, T7 secondary output voltage is just below that required to override Zener diode MR10 reference voltage and cause diodes MR8 and MR9 to conduct. If the inverter is overloaded, transformer T7 output is correspondingly higher and will cause diodes MR8 and MR9 to conduct and bias transistor VT3 to reduce the output voltage, thus protecting the inverter against overload.

13. *Over-voltage protection circuit.* A relay is included to protect external equipment against excessive supply voltage. Output from an additional winding on the power transformer T6 is rectified by diode MR11 and applied via RV2 to the base of transistor VT11. The emitter of VT11 is connected to the base of the −9V line provided by resistor R11 and Zener diode MR1, and the collector is connected via relay LRA to the −28V line. Under these conditions transistor VT11 is cut-off until the base potential reaches about −9V. The voltage from RV2 is pre-set to switch 'ON' VT11 when the inverter voltage reaches 140V, so that if the regulator loop becomes defective, the output voltage, which would normally rise to about 150V will cause RLA to operate and short-circuit part of transformer T1, via the contacts LRA/1, thus stopping the oscillator. The changeover contacts RLA/2 simultaneously complete a self-hold circuit, which cannot be broken until the d.c. supply to the inverter is disconnected.

Three-phase coupler

14. The master inverter (the unit connected to SK1) has the centre tap of its output transformer connected to the 100V tap on the output transformer of the second (slave) inverter. This connection is effected by the cross-linking of SK1 and SK2. By maintaining the 100V winding of the slave inverter at a phase angle of 90 degrees relative to the master inverter output, a 3-phase supply is made available at pins A, B and C on terminal block TB1. This supply is also connected to the blower motor. Two bridge rectifier systems are connected between the 100V slave and 115V master windings, so that any deviation from the 90 degrees phase angle between the two results in a differential d.c. voltage appearing between the rectifier outputs. When this occurs, current is driven in one direction through the series-opposing primaries of transformers T2 and T3, the secondary windings of which are series-aiding and are connected across the oscillator transformer of the slave inverter, via pins 2 and 3 of SK2. The change in inductance of transformer T2 and T3 is thus reflected into the inverter oscillator transformer in such a direction as to correct the oscillator frequency, and hence the phase of the slave inverter relative to the master unit. Transformers T2 and T3 secondaries are tuned to 400c/s by a shunt capacitor C8. In order for the inductance of the transformers to be variable in both directions, it is necessary for them to be biased under normal operating conditions; this is achieved by introducing an unbalance via the unequal feed resistors R1, RV1 and R2, the resulting bias current may be adjusted and pre-set by RV1. The two sets of opposing primary windings on T2 and T3 are necessary to permit an inductance change in both directions while providing cancellation of the a.c. voltage due to the master inverter oscillator. If this provision were not made, the 400c/s oscillator output would be reflected back into the d.c. control system and, conversely, the loading of T2 and T3 and the d.c. system would damp the master inverter oscillator. A large capacitor C9 is incorporated to isolate the secondaries of transformers T2 and T3 from the d.c. component of the oscillator current.

15. The capacitors C6 and C7 are for d.c. smoothing and resistors R3 and R4 are to reduce the time constant of the smoothing circuit, thereby reducing the loop time constant and improving loop stability. Resistor R7 and capacitor C10 also assist in improving loop stability. Series resistors R5 and R6 are to reduce the time constant of the circuit associated with the d.c. windings on transformers T2 and T3.

16. A 1:1 ratio transformer T1 is included to prevent parallel connection of diodes MR2 and MR5 and subsequent interference between the two bridge rectifiers when a common d.c. line is used. This is necessary for the correct functioning of the diode MR9, which ensures that the voltage across capacitor C7 is always greater than the voltage across capacitor C6 and that a 'latched out' condition cannot arise due to reversed saturation of the saturable transformers T2 and T3.

17. Three test sockets coded Red, White and Blue are located on top of the coupler and are connected to the output terminal A, B, and C respectively. The 3-phase output is brought to three terminals at the rear of the coupler marked A, B and C, and the phase rotation is in this sequence. The voltage between any pair of these terminals is 115V. The 28V d.c. input is fed into the inverters via terminal block TB1 and the RF suppression filter components L1, L2, C1 and C2.

18. The current limiting circuits operate in the same way to protect the inverters, but the interactions between the two circuits are complex, and the limit on each phase depends on the loading of the other two phases. The over-voltage trip operates separately for each inverter. The left-hand (viewed from the front) inverter alone determines the frequency of the system and also the voltage of the AB phase. The voltage of the other two phases depends on the voltages of both inverters and also on the setting of the control loop.

SERVICING

19. At the prescribed servicing periods or in the event of unsatisfactory performance the complete inverter assembly should be removed from its installation and serviced in accordance with the procedure given in the following paragraphs.

20. Examine the units for signs of damage, corrosion or contamination and check the security of all nuts, screws and external electrical connections.

21. Remove the twenty screws (A in fig. 2) and lift off the top cover to the extent of the cableform. Remove the four 6 B.A. csk.hd. screws (B in fig. 2) and raise the resistor tag

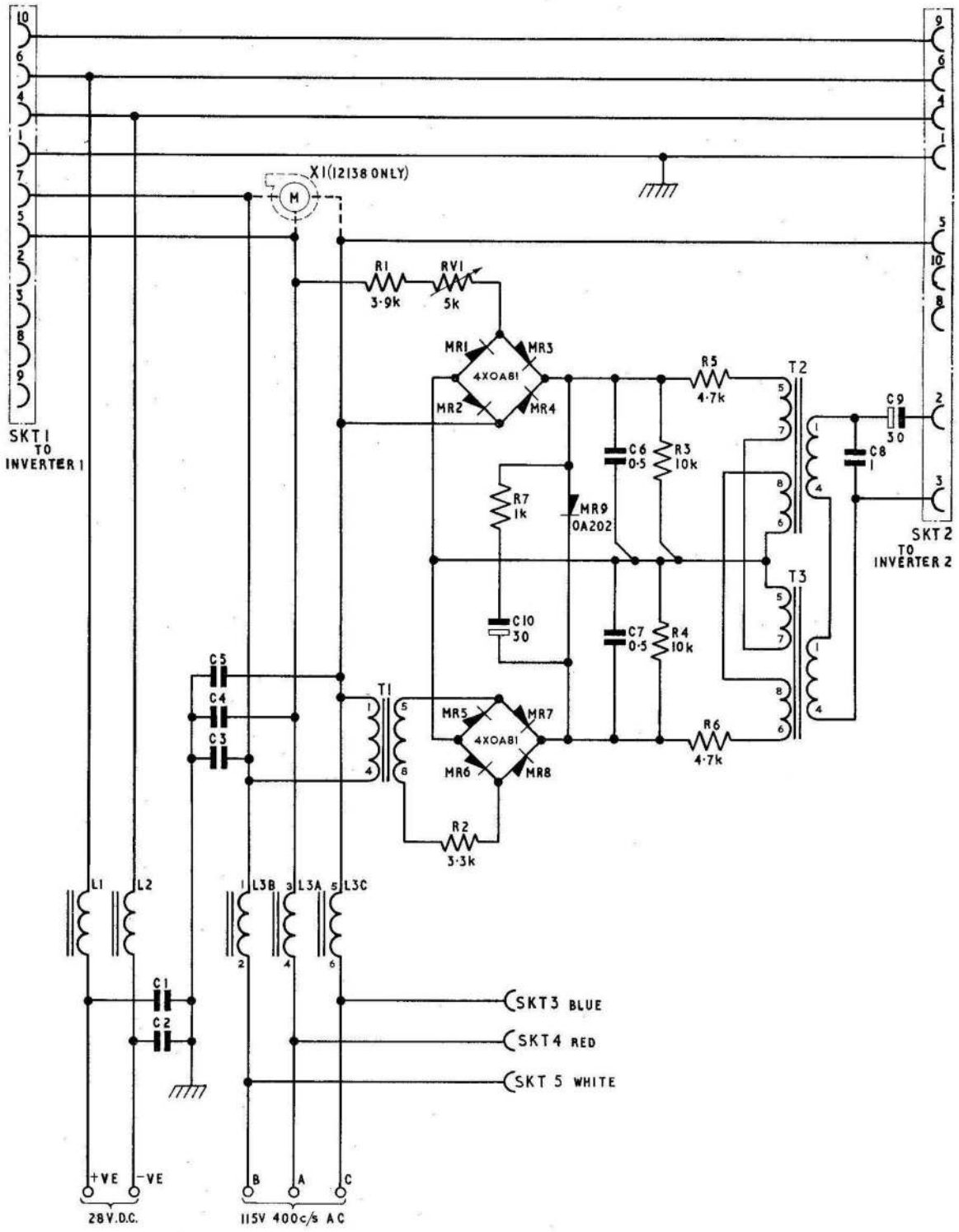

Fig. 1A. Coupler unit—circuit diagram

panel on its cableform. Remove the eight ch.hd. screws in the tray support flange to release the coupler unit from the tray. Take out the four securing screws and remove the rear cover; to obtain access to the supression components, remove the four fixing screws and the paxolin panel.

22. Remove dust from the interior of the units by blowing out with dry clean compressed air. Remove the air filter from the coupler unit and clean as required by washing in warm soapy water.

23. Examine all components for damage, cracks, fractures, corrosion or contamination. Examine all wiring for any external signs of burning or damaged insulation.

Testing

24. Details of the test which may be applied to verify the serviceability of the units will be found in Appendix A to this chapter.

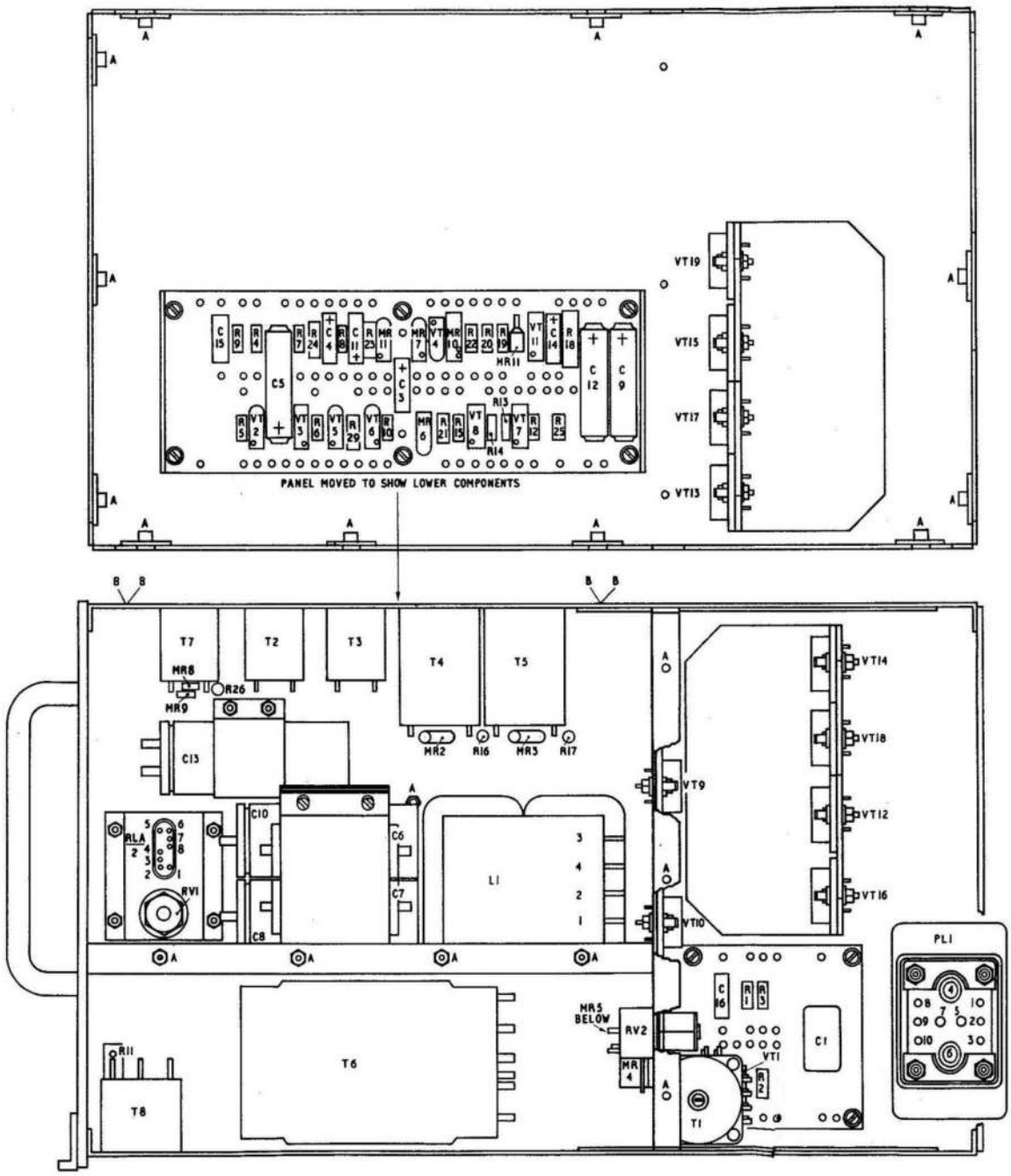

Fig.2 Inverter, Type E182, component layout Fig. 2

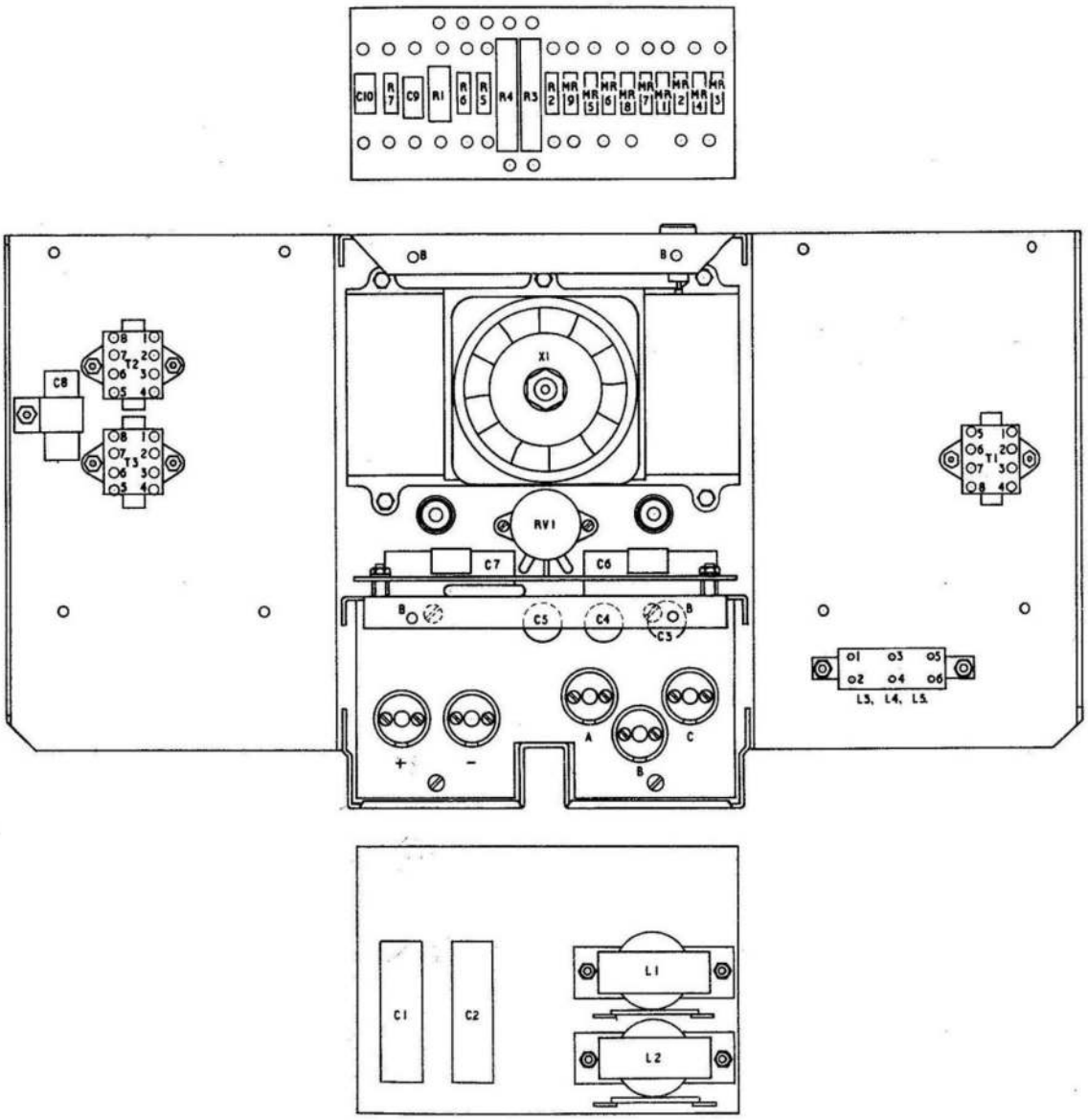

Fig.3 3-phase coupler unit, component layout Fig.3

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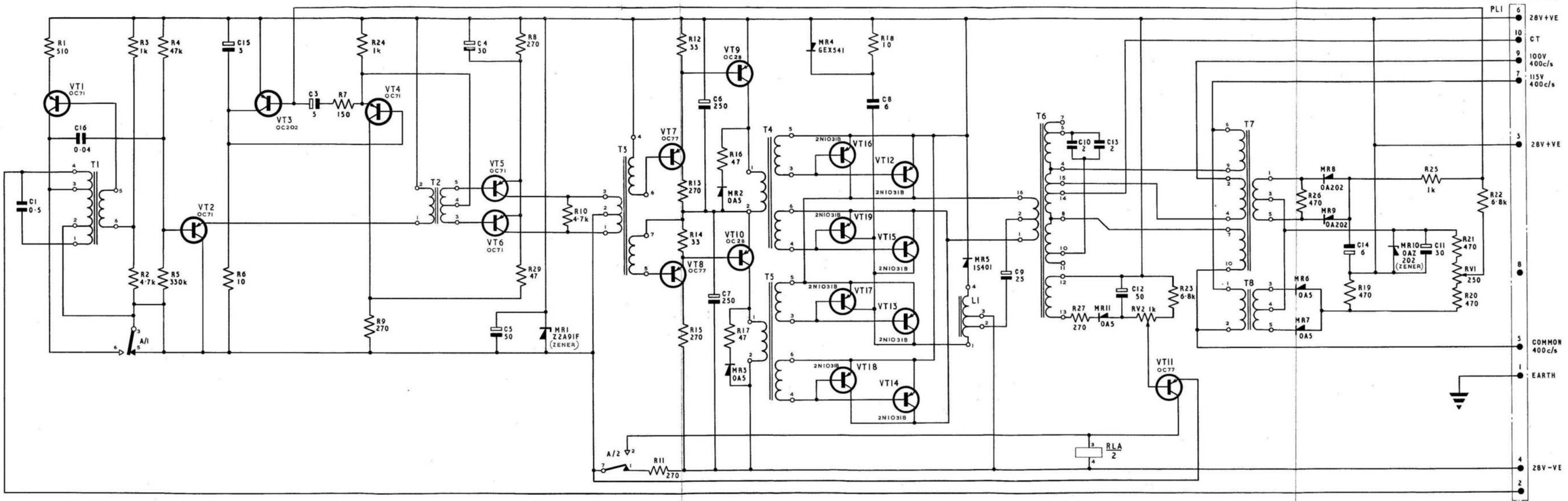

Fig. 5

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Inverter, Type E182 — circuit diagram
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Fig.5

Appendix A

STANDARD SERVICEABILITY TEST for STATIC INVERTERS, ECKO, TYPES E182 and E184/1

Introduction

1. The tests detailed in this Appendix may be applied to the inverter before it is put into service or at any time when its serviceability is suspect.

TEST EQUIPMENT AND SUPPLIES

2. The following test equipment is required.

(1) Test meter, Type D, Ref. No. 5QP/10610 (or equivalent).

(2) Frequency meter, 400 c/s.

(3) Rheostat, Non-Inductive, Triple Ganged, 37 ohm 5·6 amp. per leg (Ref. No. 5G/4712).

◀(4) Mounting tray assembly, Type M2239B (Ref. No. 5UB/8401).▶

3. It is essential that the inverter transistors are, at all times, kept below their maximum junction temperature. The output transistors are particularly critical in this respect and are mounted in good thermal contact with the outside walls of the inverter case. The temperature of each side wall, measured at points 9 in. from the front panel and 5 in. from the base, that is, approximately in the centre of the group of rivets, must not exceed 65 degrees C.

4. The d.c. supply used for the following tests should not be from a rectified source unless shunted by a capacitor, of value not less than 5,000 μF, across its output terminals. Capacitor 5,000 μF 50V d.c. (Ref. No. 0631-5910-99-580-2011) or equivalent is suitable.

Caution . . .

It is essential that the supply polarity is observed, as reversed polarity connection will result in immediate destruction of the output transistors.

Method

5. The individual inverters, Type E182 should be tested and adjusted separately as follows:—

(1) Connect a 28V d.c. supply to pins 4 and 6 on the Cannon plug and measure the a.c. output voltage and frequency at pins 5 and 7. The voltage should be 115V a.c. and the frequency 400 c/s when tested at an ambient temperature of 20 degrees to 30 degrees C.

(2) Connect a 28V d.c. supply to pins 4 and 6 and check that the voltage is 115V a.c. at pins 5 and 7. Connect 75 ohm resistance across pins 5 and 7 and observe the change of output voltage. This should be not greater than 2V r.m.s.

(3) Check the overload characteristics as follows:—

(a) With a 28V d.c. supply connected to pins 4 and 6 connect 30 ohm resistance across pins 5 and 7 and measure the voltage. This should be not greater than 70V a.c.

(b) Repeat the foregoing test with 25 ohm resistance connected across pins 5 and 9. The voltage should be not greater than 70V a.c.

(4) Check the operation of the over-voltage trip circuit by increasing the output voltage by means of RV1 until the unit trips. The voltage at which this occurs should be 140V $\pm$ 2V. Adjust potentiometer RV1 so that the output voltage is 115V a.c. Access to RV1 is gained by removing the cover (para. 21), RV1 is located behind the front panel.

6. Insert the two type E182 inverters in the mounting tray. Connect a 28V d.c. supply to the input terminals on the rear terminal board. Adjust the a.c. output voltage by means of the phase setting control potentiometer RV1, using the trimming tool provided, so that equal voltages are obtained between terminals C—A and C—B. The potentiometer RV1 is located immediately behind the front panel of the 3-phase coupler unit; the control spindle is accessible through an aperture in the front panel between two inverters. This adjustment should be made at no load or with the load at which the inverter is to be used.

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Appendix 1

STATIC INVERTER, ECKO, TYPE E184/1

LEADING PARTICULARS

*Static inverter, Ecko, Type E*184/1	*Ref. No. 5UB*/8328
Input	
Voltage	23*V to* 28·5*V d.c.*
Power (no load)	55*W*
Output	
Voltage	115*V a.c.* ± 2 *per cent, 3-phase*
Frequency	400 c/s ± 1 *per cent*
Power	300*VA*
Power factor (with balanced load)...	0·5 *lagging to* 0·8 *leading*
Weight (approx.)	23 *lb.*

Introduction

1. The static inverter, Ecko, Type E184/1 is described and illustrated in the main Chapter.

Appendix 2

STATIC INVERTER, ECKO, TYPE E182

LEADING PARTICULARS

*Static inverter, Ecko, Type E*182	*Ref. No. 5UB/*8329
Input	
Voltage	23*V to* 28·5*V d.c.*
Power (no load)	31*W*
Output	
Voltage	115*V a.c.* ± 2 *per cent, single phase*
Frequency	400 *c/s* ± 1 *per cent*
Power	150*VA*
Power factor	0·5 *lagging to* 0·8 *leading*
Weight	8½ *lb.*

Introduction

1. The static inverter, Ecko, Type E182 forms part of the composite unit Type E184/1 described and illustrated in the main Chapter. The single inverter is fitted in a mounting rack which incorporates a radio interference suppression unit. Cooling air to the inverter is provided by an axial fan fitted to the mounting rack and supplied from the single phase output. External connections are made to four No. 10 U.N.F. terminals accessible under the rear cover.

2. Details of servicing and testing procedures are given in the main Chapter and Appendix A.

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