Cancelled now 1BF-0402-1

Chapter 2

AMPLIFIER UNIT, SMITHS TYPE EC4/4

LIST OF CONTENTS

LIST OF ILLUSTRATIONS

LEADING PARTICULARS

Amplifier unit, Smiths Type EC.4/4	*Ref. No. 5CZ/5543*
Input voltage	115*V*, 3-*ph*., 400 *c/s*.

Introduction

1. The jet-pipe temperature control amplifier, Type EC4/4, is designed to control the fuel flow in of an aircraft jet engine, so that the jet-pipe temperature is controlled at an optimum value. In response to a signal from thermocouples, located in the jet-pipe, the amplifier output energises one of a pair of relays, depending on the sense of the signal, to run an actuator motor and hence increase or decrease the fuel flow to the engine.

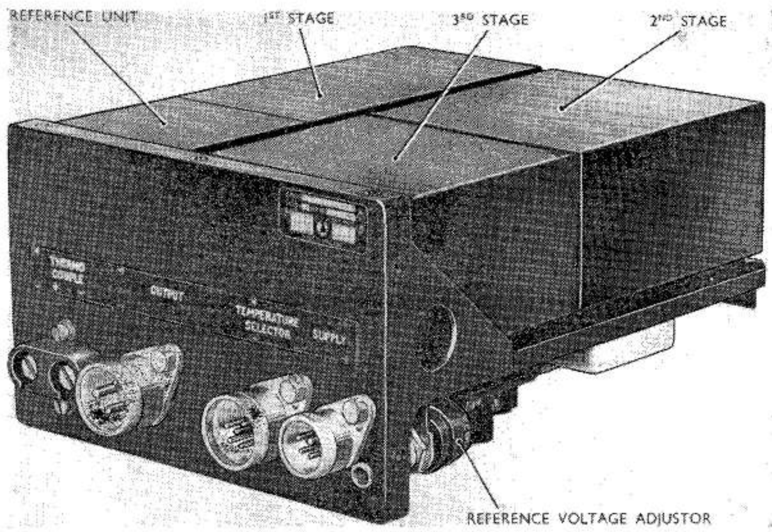

Fig 1. Amplifier Unit EC4/4

DESCRIPTION

2. The components are mounted on a fabricated aluminium alloy chassis which is attached to the front panel. The three amplifier stages and the reference unit are contained in sealed metal canisters mounted above the chassis (*fig*. 1) and the output stage rectifiers, relays, capacitors and resistors below the chassis (*fig*. 2). The cold junction compensating resistor is wound on the thermo couple terminal assembly on the front panel; the terminal assembly forming the cold junction of the system. The variable resistor RV1, for adjusting the reference voltage, is located behind the front panel and has a slotted spindle, which is accessible through the panel, for screw-driver adjustment.

OPERATION

Reference voltage

3. The reference voltage is derived from a resistance bridge, which is supplied from a stabilized voltage source. The stabilizing network is also a bridge arrangement with a neon tube V1 forming one arm of the bridge (*fig*. 6). The output from the reference bridge (the reference voltage) is connected in opposition to the thermocouple e.m.f. and when the two e.m.f.'s are equal there is no signal fed into the amplifier. The output from the bridge and hence the datum temperature may be adjusted by potentiometer RV1.

Amplifying stages

4. Any difference in the thermocouple and reference voltages results in a current flowing in the two control windings of transductor X1, via choke L1, in the first stage amplifier. The phase transductor X2 is controlled by a steady d.c. bias, obtained from the rectifier bridge MR2 via resistor R15. Choke L1 and resistor R15 are included to suppress the second harmonic currents which are induced into the control windings by the main exciting winding.

5. The exciting windings of the two transductors are connected in series and supplied from transformer TR1 via capacitor C1. The output from the stage is supplied by an additional winding of transductor X1, into which currents are induced by the main exciting winding at double the supply frequency (second harmonic). The output is rectified by a phase sensitive rectifier comprising MR3-6 and the d.c. output is developed across R23. The reference voltage for the phase sensitive rectifier is supplied by the output windings of transductor X2, which are loaded by resistor R20. Thus transductor X2 with its steady bias produces a steady a.c. signal across R20, and the output of transductor X1 is also an a.c. signal, but varies in phase and magnitude as the control current varies. The two signals, which are both at double the supply frequency are mixed at the bridge network and the resultant rectified signal appears across R23. In this way the sense of

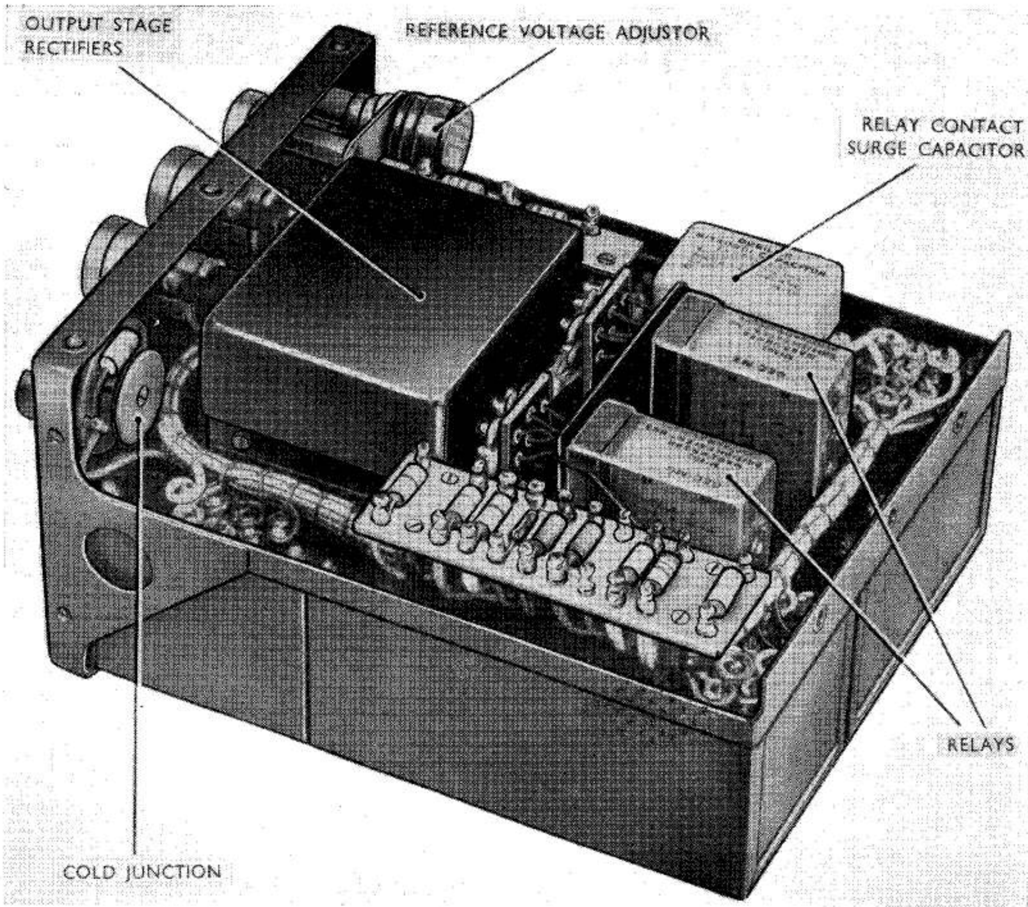

Fig 2. Underside of Amplifier

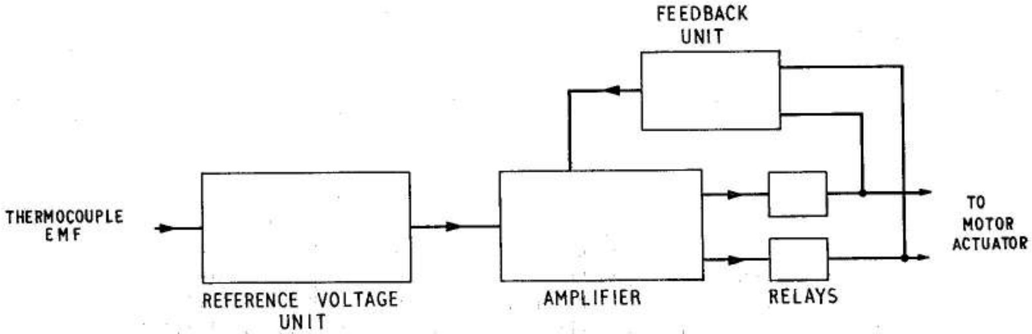

Fig 3. Block diagram

the input signal is preserved. Feedback to the stage is provided by voltage developed across the network comprising R21, R22 and TH.1.

6. The output of the first stage is applied to the control windings of the intermediate stage, via smoothing circuit L3. This stage comprises two auto-self-excited transductors connected in a push-pull arrangement with series mixing and self-bias windings. The output voltage is developed across balance resistors R27 and R28 and applied to the control winding of the output stage, via resistor R25 and smoothing network L4, L5 and C5. The voltage developed across R25 is applied to the stage as negative feedback.

7. The output stage consists of two transductors each connected, via rectifiers, to the operating coil of an associated relay. The transductors are biased in the opposite sense by windings supplied from the same d.c. source which feeds the reference bridge. Each relay operates three pairs of contacts ; one to complete the supply to the drive motor, in one direction ; one to open the circuit to the motor in the opposite direction (interlock contacts) ; and one to switch in a feedback circuit.

Feedback

8. When the relay operates the feedback contacts cause a fixed voltage to be injected into the second stage input circuit ; the polarity of the feedback voltage depends on which relay is operating, and is arranged to oppose the input. When the relay operates on a weak signal, the feedback voltage will reduce the input sufficiently to open the relay again. A strong signal on the other hand will not be reduced sufficiently by feedback to open the relay. The actuator motor mean speed is thus governed by the strength of the signal, the feedback causing the relay to vibrate on and off, with the duration of 'on' periods depending on the strength of the input signal.

SERVICING

Testing

9. The following equipment is required to test the datum temperature, inactive zone and feedback range :—

(1) Test equipment Ultra, Type QE2230
(2) Bench test ring made up as shown in fig. 4
(3) 115V, 3-phase, 400c/s supply
(4) Stop watch
(5) Temperature selector plug

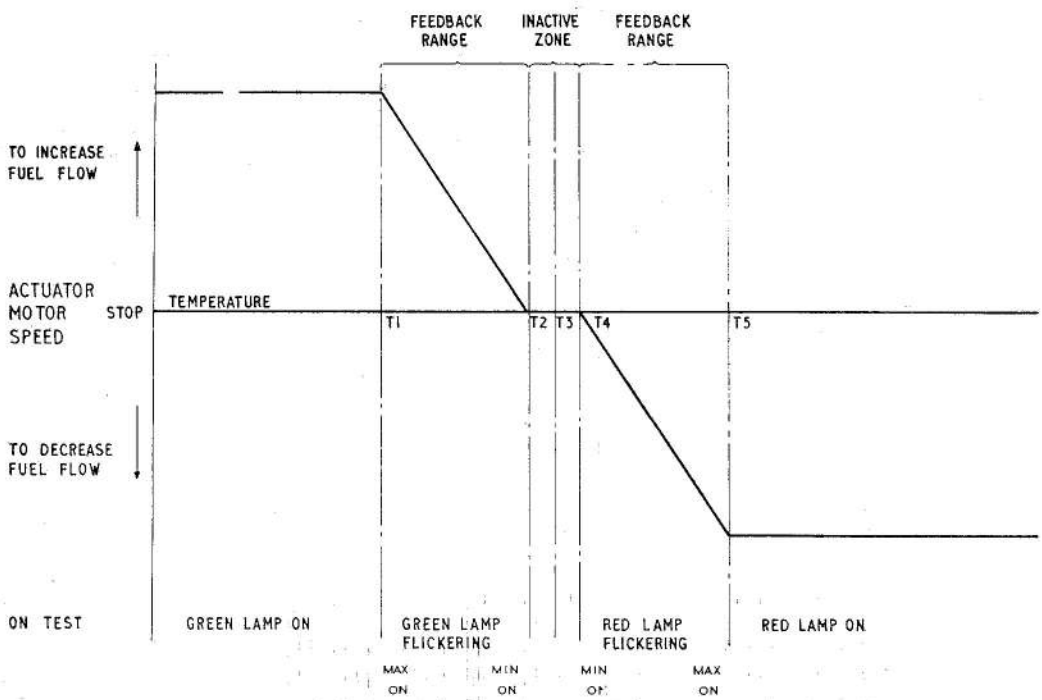

Fig. 4. Response curve

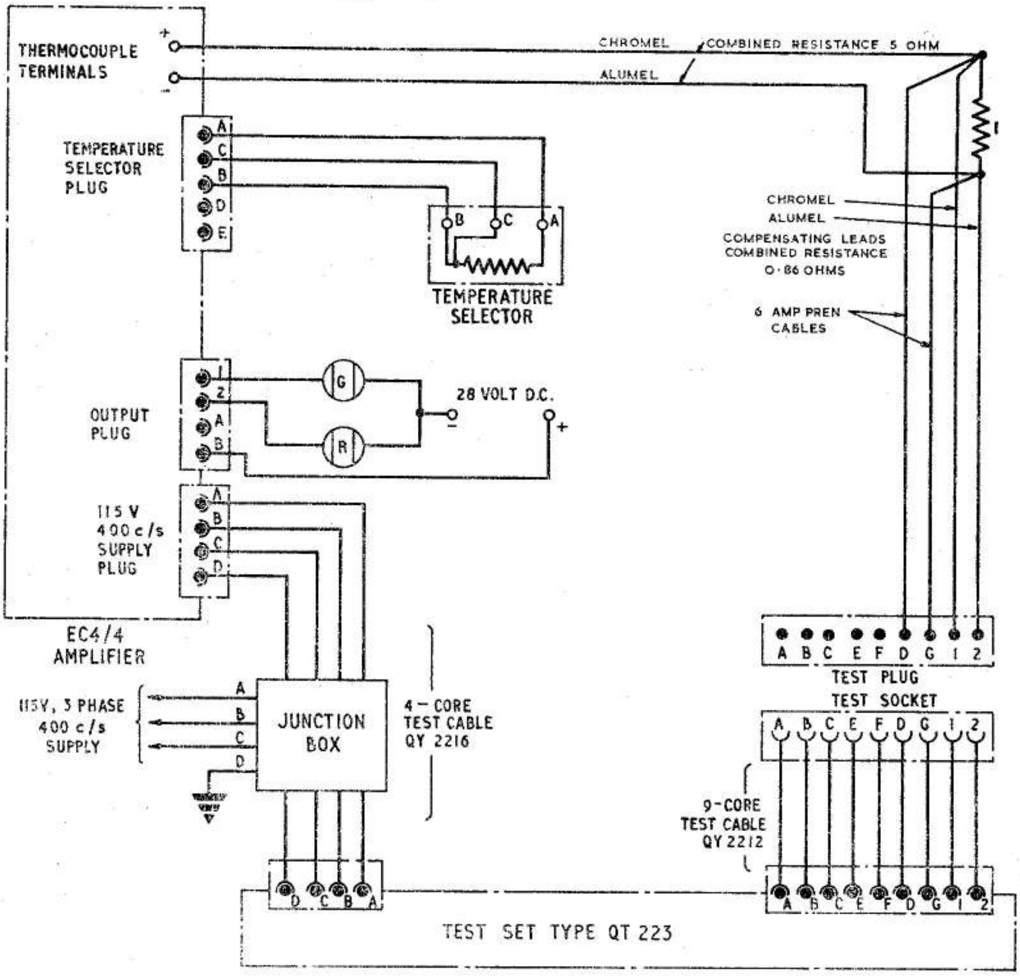

Fig 5. Test Circuit

Preparation

10. Check the test set batteries and power supplies as described in Sect. 10, Chap. 1 (Bench Testing) of this publication, remove test cable QY2216 and connect 115V supply direct to amplifier. Inject simulated temperature signal until red light is continuously on, and allow 30 minutes for amplifier to warm up.

Datum temperature

11. To establish datum temperature proceed as follows :—

(1) Reduce simulated temperature signal until green indicator lights.

(2) Increase temperature signal slowly using coarse and fine controls until green lamp just ceases to flicker (T2, *fig.* 5). Measure simulated temperature signal.

Note . . .

Instructions for operating Ultra test equipment QE2230 to inject and measure temperature signals are given in Sec. 10, Chap. 1 of this publication.

(3) Further increase the temperature signal until red light starts to flicker, and then using the fine control reduce temperature signal until red light just ceases to flicker (T4, *fig.* 5). Again measure the simulated temperature signal.

(4) The datum temperature, i.e. mid-point of the inactive zone (T3, *fig*. 5) is the mean of the two temperature readings. The inactive zone is given by T4—T2 and should be between 6 and 8°C.

Feedback range

12. Check the feedback range as follows:—

(1) Adjust the temperature signal until the red light is at the point of commencing to flicker (T4), and measure the simulated temperature.

(2) Further increase the applied signal until the red lamp is just lit continuously (T5), and again measure temperature. The difference between the two readings (T5—T4) should be 25 to 30°C.

(3) Repeat the procedure for the green light flickering zone, T2—T1 should be 25 to 30°C.

Insulation resistance

13. Measure the d.c. insulation resistance between the following points using 500 V insulation resistance tester. The resistance should not be less than 5 megohms.

(1) Thermocouple +ve terminal and chassis.

(2) Thermocouple +ve terminal and supply plug pole A.

(3) Supply plug pole A and chassis.
(4) Output plug pole B and chassis.
(5) Output plug pole 1 and chassis.
(6) Output plug pole 2 and chassis.

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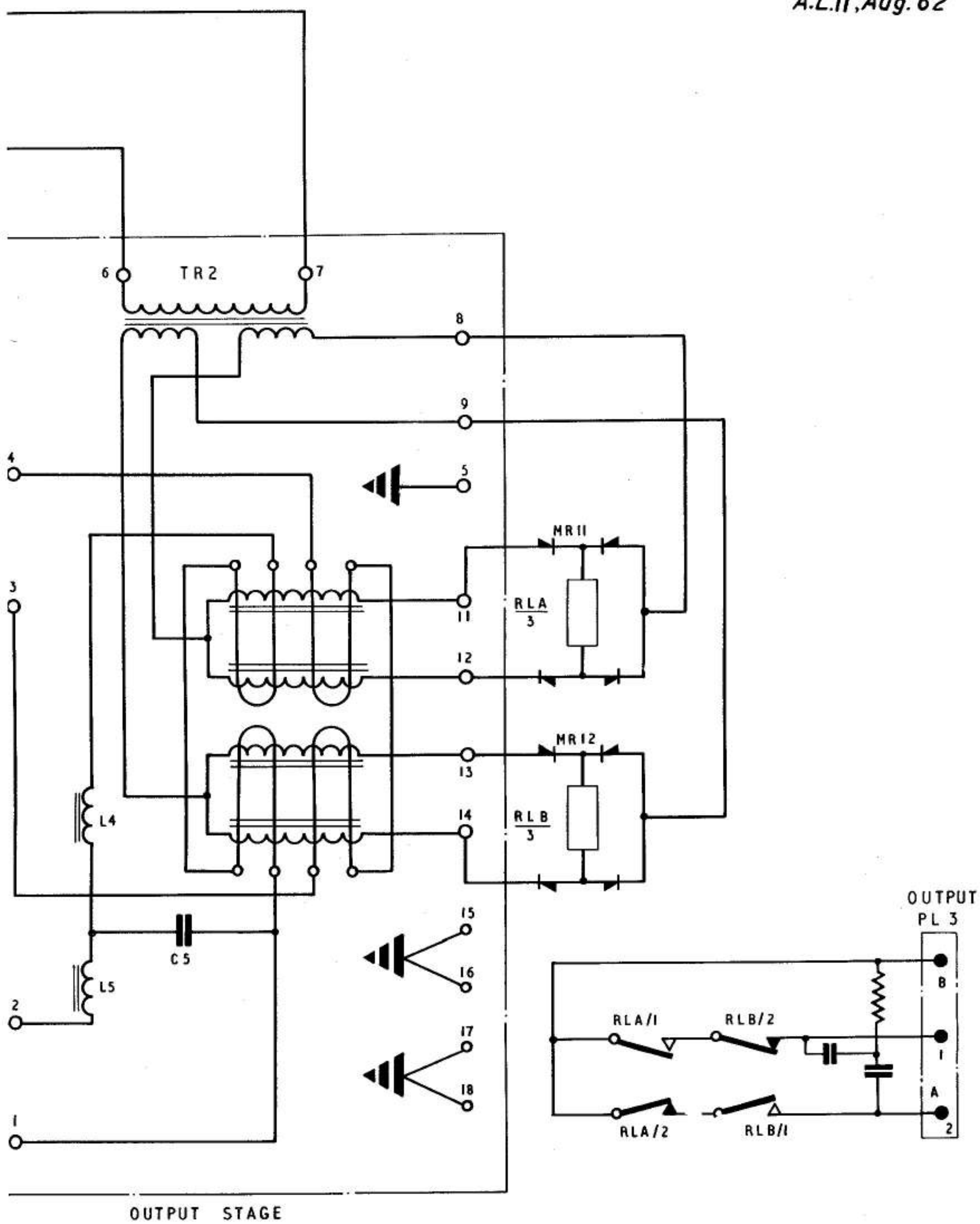
TR2
6
7
8
9
4
5
3
MR11
RLA
3
11
12
MR12
13
14
RLB
3
L4
C5
L5
2
1
15
16
17
18
OUTPUT
PL 3
B
1
A
2
RLA/1
RLB/2
RLA/2
RLB/1
OUTPUT STAGE

Fig. 6

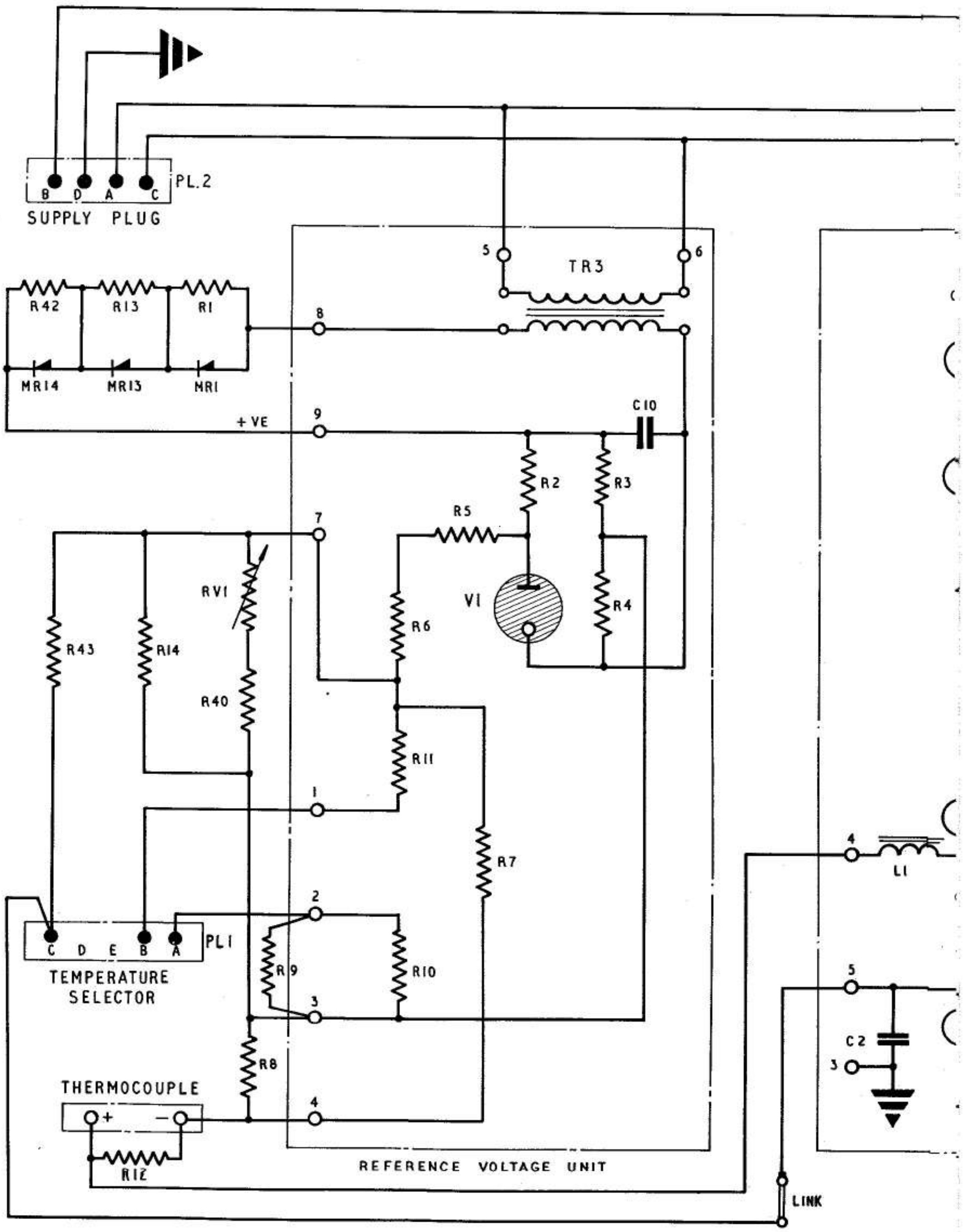

Fig. 6

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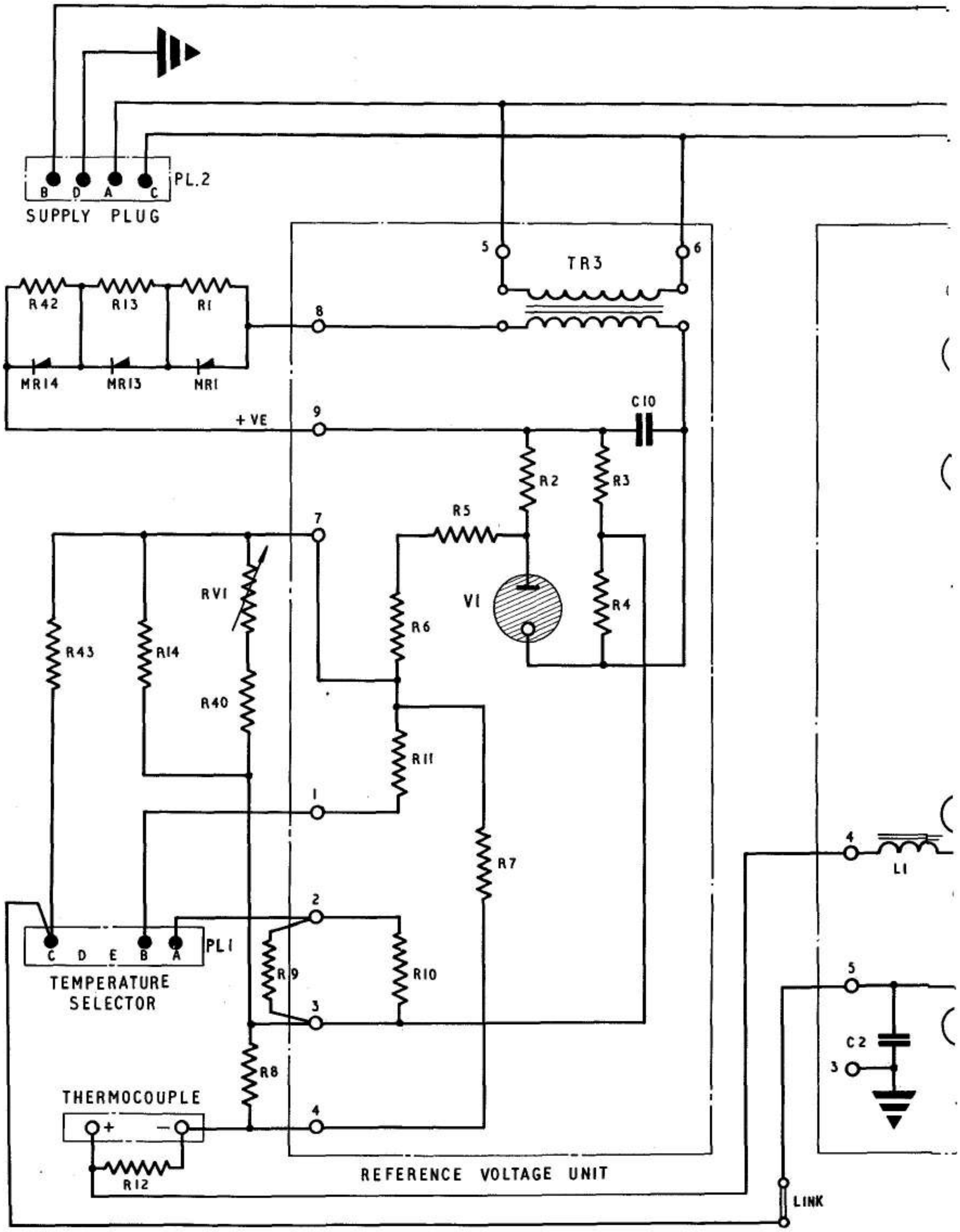

Fig. 6

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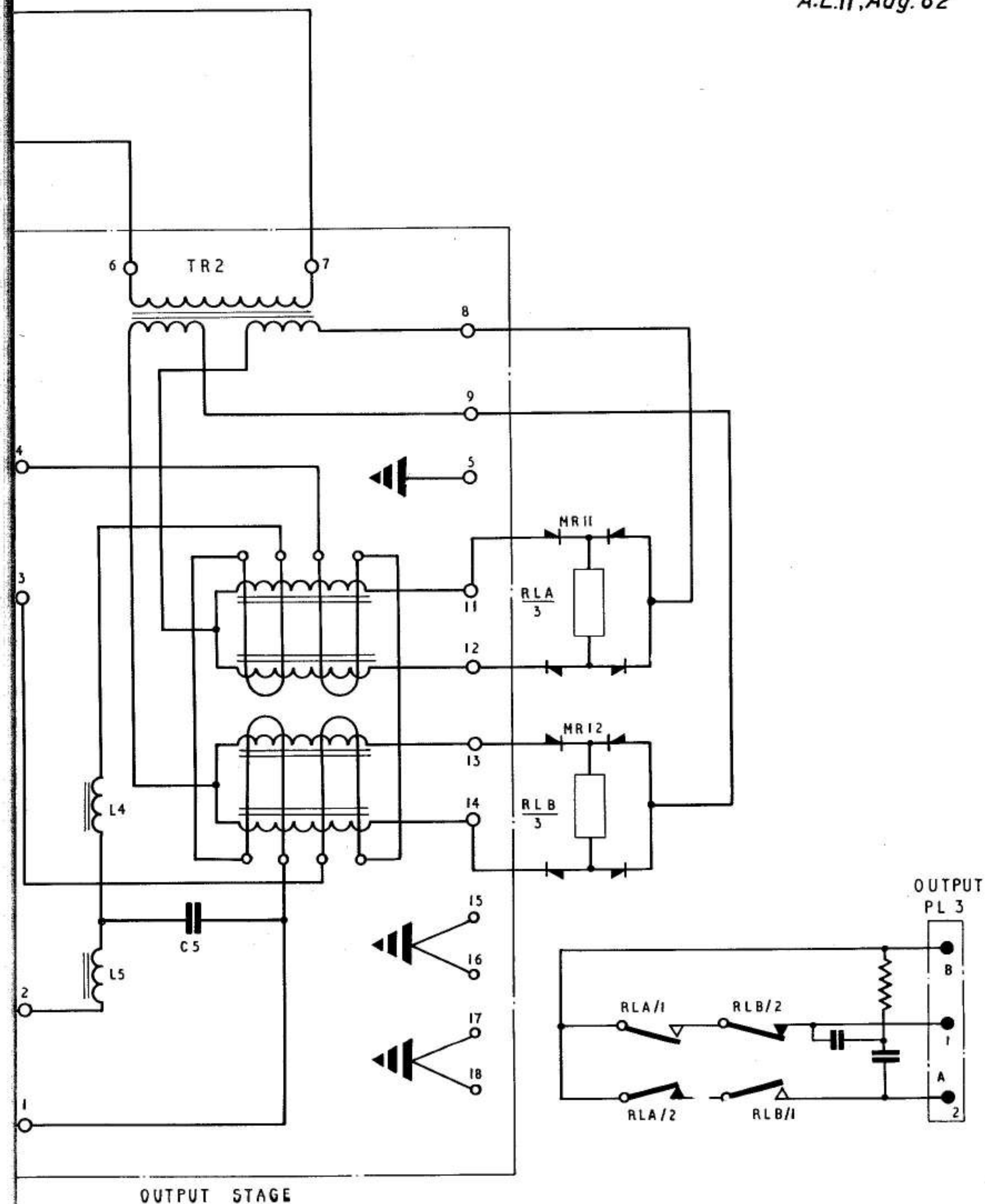
TR2
6
7
8
9
4
5
3
MR11
11
RLA
3
12
MR12
13
RLB
3
14
L4
C5
L5
15
16
17
18
2
1
OUTPUT
PL 3
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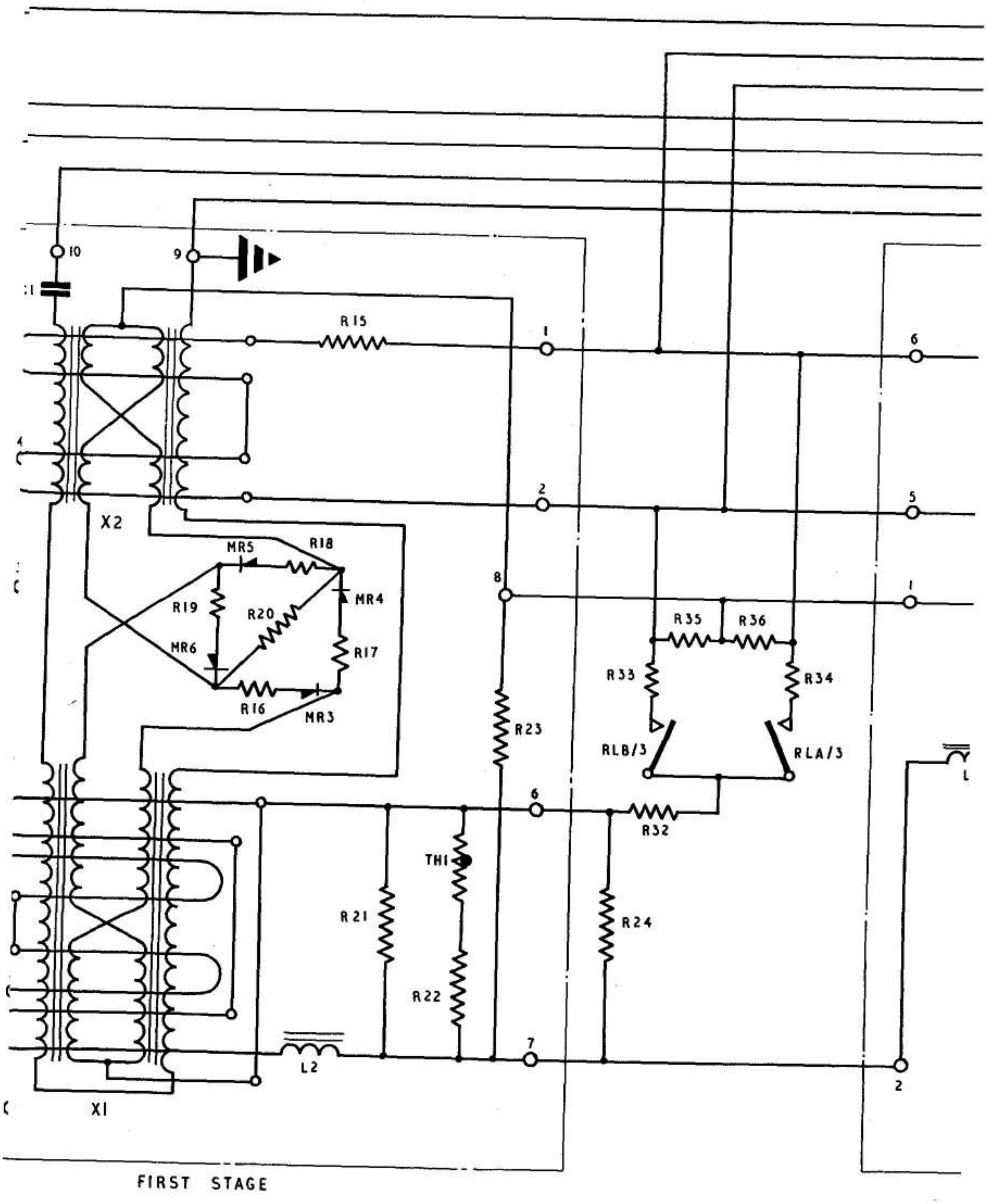
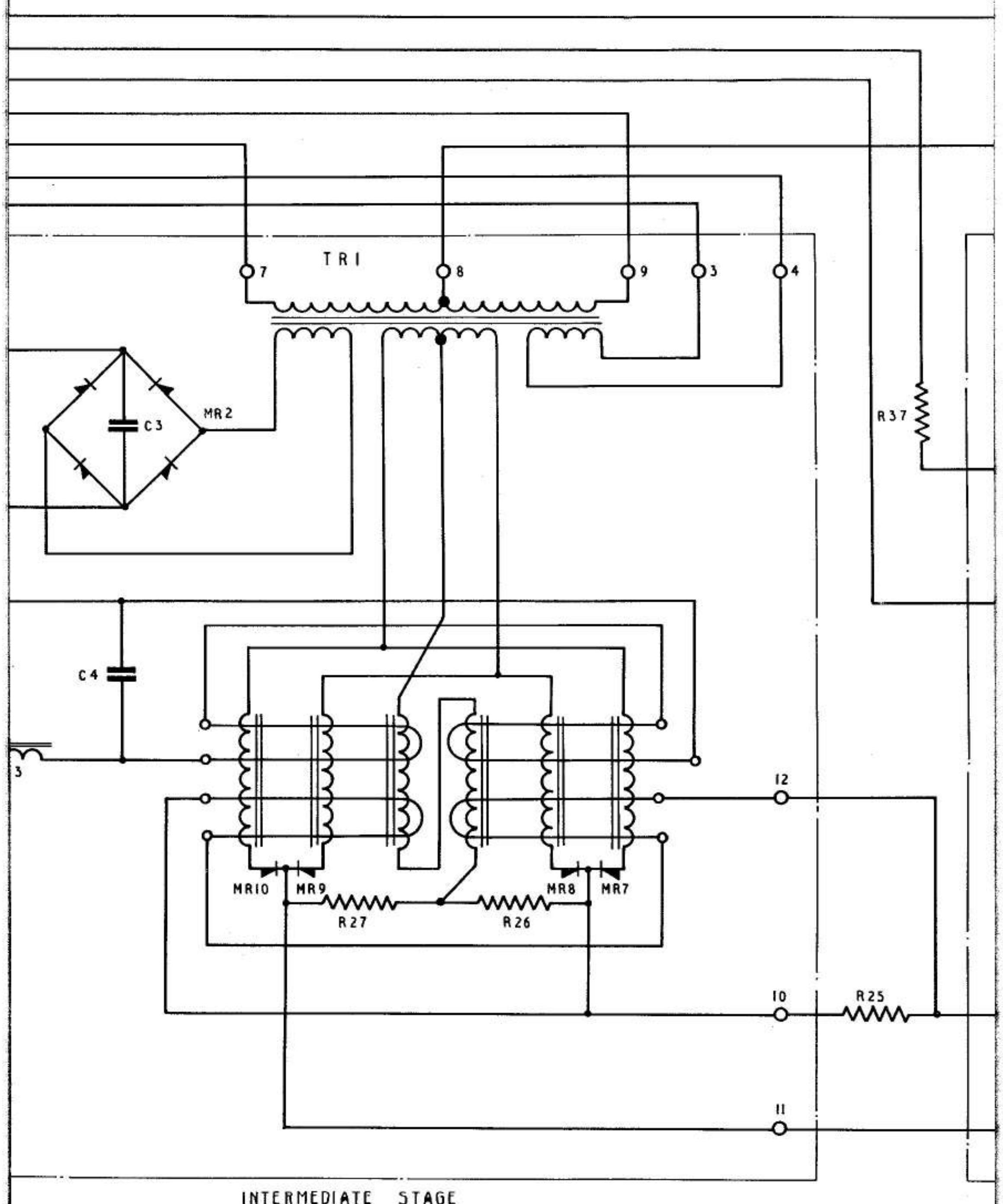
RLA/1
RLB/2
1
A
RLA/2
RLB/1
2
OUTPUT STAGE

Fig. 6



Circuit di

R E S T R I


TR1
7
8
9
3
4
MR2
C3
R37
C4
3
12
MR10
MR9
MR8
MR7
R27
R26
10
R25
11
INTERMEDIATE STAGE

agram

C T E D


LTF
RAF BINBROOK